REMARKS

The application includes claims 2, 4-17, and 19-31 prior to entering this amendment.

The examiner rejects claims 2, 4-17 and 19-31 under 35 U.S.C. § 103(a) as being unpatentable over Grisamore (U.S. Patent 6,535,901) in view of Yamazaki et al. (U.S. Patent 4,706,211).

The examiner rejects claims 2, 4-17 and 19-31 under 35 U.S.C. § 103(a) as being unpatentable over Costa et al. (U.S. Patent 5,935,201) in view of Yamazaki et al.

In the present amendment, the applicants cancel 4, 6, 19, and 21, amend claims 2, 5, 7-10, 12, 14, 17, 20, and 22-31, and add new claims 32-37. Thus, claims 2, 5, 7-17, 20, and 22-37 are now pending after entering this amendment. Applicants respectfully request reconsideration of all pending claims in view of the arguments presented below.

Claim Amendments

The applicants amend claims 2, 5, 7-10, 12, 14, 17, 20, and 22-31 and add new claims 32-37. Support for the new and amended claims may be found in the specification as filed, for example, on pages 9-14 and FIGs. 2-6. No new matter has been added.

Claim Rejections Under § 103

A. Dynamic reallocation in claims 2 and 17

As amended, claim 2 includes "selecting atomic elements of a dedicated logic device in which to implement the Wallace-architecture of full-adders, half-adders, and associated registers; and selecting atomic elements to implement control logic, the control logic configured to dynamically reallocate the atomic elements implementing the Wallace-architecture of full-adders, half-adders, and associated registers in response to subsequent analysis of the input terms on a bit-wise basis." Claim 17 includes similar language.

In contrast, neither the combination of Grisamore and Yamazaki, nor the combination of Costa and Yamazaki teach or suggest such dynamic reallocation of atomic elements. For example, although Grisamore describes the generation of a fast multiply accumulation circuit, there is no mention that the fast multiply accumulation circuit can be dynamically reallocated once the fast multiply accumulation circuit is generated.[1] Costa describes a multiplier circuit

[1] Grisamore, Abstract.

itself, not its reallocation.[2] Similarly, Yamazaki describes a digital multiplying circuit, not the reallocation of its elements.[3] Accordingly, neither the combination of Grisamore and Yamazaki, nor the combination of Costa and Yamazaki teach or suggest each and every element of claims 2, 17, and dependent claims 5, 7-16, 20, and 22-31. The applicants request that the examiner withdraw the rejection of claims 2, 5, 7-17, 20, and 22-31.

B. Hyperpipelining in claims 2 and 17

Claim 2 recites that "a hyperpipelined series of Boolean function generators is to implement a Wallace-architecture of full-adders ..., half-adders ..., associated registers." Accordingly, it is the Wallace-architecture that is pipelined. Claim 17 includes similar elements.

The examiner has alleged that it would have been obvious to "provide the Wallace-architecture of Grisamore with registers at optimal points in the architecture to enable pipelined processing." The reduction tree module 14 in Grisamore can be a Dadda tree reduction module or a Wallace tree reduction module.[4] Hence, the modification of Grisamore to add pipelining to the Wallace-architecture would add pipelining to the reduction tree module 14.

Such a modification directly conflicts with the operation of Grisamore. For example, the first and second preceding resultants 26 and 28 are combined with the current partial products 24 to generate the first and second current resultants 30 and 32 in the reduction tree module 14.[5] The first and second current resultants 30 and 32 are used in the next cycle as the first and second preceding resultants 26 and 28.[6] Each cycle, the current resultants are fed back to the reduction tree module 14 as the preceding resultants.

As a result, there cannot be registers within the reduction tree module 14 for pipelining. If there were, the preceding resultants 26 and 28 that are fed back would be delayed by the number of cycles that it takes to pass through the pipelined reduction tree module 14. The first and second current resultants 30 and 32 would no longer be used in the next cycle as the first and second preceding resultants 26 and 28, but a number of cycles equal to the depth of the pipelining. Accordingly, one skilled in the art would not add pipelining registers to the reduction tree module 14 of Grisamore. The combination of Grisamore and Yamazaki does not teach or

[2] Costa, col. 2, line 66 – col. 3, line 18.
[3] Yamazaki, col. 3, ll. 12-17.
[4] Grisamore, col. 2, ll. 66-67.
[5] Grisamore, FIG. 1 and col. 3, ll. 27-42.

suggest each and every element of claims 2, 17, and dependent claims 5, 7-16, 20, and 22-31. The applicants request that the examiner withdraw the rejection of claims 2, 5, 7-17, 20, and 22-31.

C. New claims 32-37

Claim 32 includes "designing the hyperpipelined series of Boolean function generators to implement the multi-input adder in a pipeline stage of the hyperpipelined series of Boolean function generators immediately after a final pipeline stage of full-adders, half-adders, and/or registers."

As described above, pipelining would not be added to Grisamore. Hence, the combination of Grisamore and Yamazaki does not describe a final pipeline stage, immediately after which the multi-input adder is implemented.

In the combination of Costa and Yamazaki the adder is several pipeline stages removed from the multiplier. Two pipeline registers separate the multiplier 60 from the adder 62.[7] There is no suggestion to remove the two pipeline registers, the 16 bit lookahead adder and the arithmetic shifter in the arithmetic unit 48 of Costa to have the 32 bit adder 62 and accumulator register immediately after the 8x8 multiplier 60.

Accordingly, neither the combination of Grisamore and Yamazaki, nor the combination of Costa and Yamazaki teach or suggest each and every element of claim 32.

Claim 33 includes selecting atomic elements to implement a first combinatorial module, the first combinatorial module to generate partial products of real components of a plurality of complex numbers; and selecting atomic elements to implement a second combinatorial module, the second combinatorial module to generate partial products of imaginary components of the complex numbers." In addition claim 33 recites that "the partial products of the combinatorial modules form the input terms." Accordingly, the input terms that are analyzed and combined in the hyperpipelined series of Boolean function generators are partial products from two multiplications. Claim 34 adds additional combinatorial modules for additional partial products.

As can be seen every figure of Yamazaki, the output of register X 1 and register Y 1 are input to generate the output register X*Y 17. Similarly, Costa only describes the multiplication

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[6] Grisamore, col. 3, ll. 2-4.
[7] See Costa, FIG. 9.

of two factors A and B.[8] In Grisamore, the inputs to the reduction tree 14 are partial products 24 and the first and second preceding resultants 26 and 28. Grisamore, FIG. 1. The first and second preceding resultants 26 and 28 are not partial products, but results of the summation of the partial products 24 from a preceding cycle. Thus, none of Grisamore, Costa, or Yamazaki describe two sets of partial products being combined in the same block.

Claim 35 includes "control elements to dynamically reallocate a plurality of atomic elements forming at least one of the hybrid summing module and the adder in response to an analysis of the partial products." As described above, neither the combination of Grisamore and Yamazaki, nor the combination of Costa and Yamazaki teach or suggest the dynamic reallocation of atomic elements.

Claim 36 includes "a first combinatorial module to generate a first portion of the partial products in response to a first input and a second input; and a second combinatorial module to generate a second portion of the partial products in response to a third input and a fourth input." Accordingly, the partial products input to the hybrid summing module include portions from the combination of two different sets of inputs. In contrast, As described above, Costa focuses on the multiplication of two inputs (X and Y), and Grisamore only describes one set of partial products 24. Thus, neither the combination of Grisamore and Yamazaki, nor the combination of Costa and Yamazaki teach or suggest two combinatorial modules of claim 36..

Claim 37 includes "a third combinatorial module to generate a first portion of a second plurality of partial products in response to the first input and the fourth input; a fourth combinatorial module to generate a second portion of the second plurality of partial products in response to the second input and the third input; a second hybrid summing module to combine a plurality of partial products into a plurality of intermediate summation results; and an second adder to add the intermediate summation results. Thus, claim 37 includes two additional combinatorial modules with the same inputs as the first two combinatorial modules, but with the inputs grouped differently. No such multiple combinatorial modules are suggested in Grisamore or Costa.

Accordingly, neither the combination of Grisamore and Yamazaki, nor the combination of Costa and Yamazaki teach or suggest each and every element of claims 33-37.

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[8] Costa, col. 4.

Conclusion

For the foregoing reasons, the applicants request reconsideration and allowance of the remaining claims. The applicants encourage the examiner to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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Respectfully submitted,

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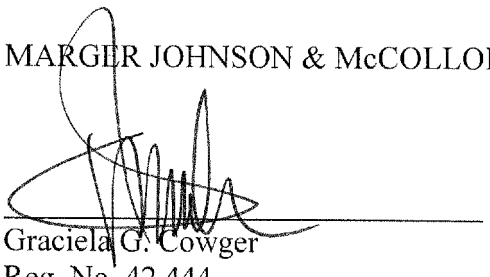

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